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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,677	12/14/1998	HYUN CHANG LEE	8733D-7153	9588

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EXAMINER
NGUYEN, KEVIN M

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 07/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/211,677	LEE, HYUN CHANG	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *17,18* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 2/14/2002 is entered. The rejections of claims 1-26 are maintained.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasui et al (US 5,784,039).

As claim 1, Yasui et al teaches an active matrix liquid crystal display device having a plurality of pixels Lij (figure 1B), a source driver 2 connecting to n columns of source driver Si-Sn, and a gate driver 3 connecting to m+1 rows of gate buses Gi-Gm+1 (col. 4, lines 31-33).

The gate high voltage V_{GH} applies a first voltage to the gate signal line Gi (figure 3A, col. 6, lines 1-45), the gate low voltage V_{GL} applied a second voltage to the gate line

Gi sequentially (figure 3B, col. 6, lines 46-58), the gate driver 3 supplied the gate buses G1, G2, ...,Gm+1 one after another with pulse-like scanning voltages Vg1, VG2, ...,VGm+1 one horizontal scanning period H and are sequentially displaced one horizontal scanning period apart in phase (col.4, lines 53-59). In figure 7, it is also possible to generate voltage K1 (Vx1+Vx2) and K2 (Vx1-Vx2) from the first and second voltage variable voltage source 6 and 7. It must be noted that the bias voltage Vx1 and Vx2 are provided immediately prior to the application of the gate select level V_{GH} (a first gate voltage changing prior to exiting of successive gate signal lines as claimed, col. 4, lines 15-17).

An equivalent circuit diagram for explaining the migration of charges at the time when a TFT is in the ON state in Fig. 1B (the first gate voltage has a voltage level that turns on the switching transistor as claimed, col. 3, lines 46-48). An equivalent circuit diagram for explaining the migration of changes at the time when the TFT is in the OFF state in Fig. 1B (the second gate voltage has a voltage level that turns off the switching transistor as claimed, col. 3, lines 49-51).

As to claims 2-6, Yasui et al teaches figure 9 having a waveform VGH and VGL rise and fall times at leading and trailing edges of the gate pulse and the second bias voltage, respectively in Fig. 8A (col. 4, lines 15-17).

As to claims 7-9, Yasui et al teaches a method for an active matrix liquid crystal display device having a plurality of pixels Lij (figure 1B), a source driver 2 connecting to n columns of source driver Si-Sn, and a gate driver 3 (shift register) connecting to m+1 rows of gate buses Gi-Gm+1 (col. 4, lines 31-33).

An equivalent circuit diagram for explaining the migration of charges at the time when a TFT is in the ON state in Fig. 1B (the first gate voltage has a voltage level that turns on the switching transistor as claimed, col. 3, lines 46-48). An equivalent circuit diagram for explaining the migration of changes at the time when the TFT is in the OFF state in Fig. 1B (the second gate voltage has a voltage level that turns off the switching transistor as claimed, col. 3, lines 49-51).

The gate high voltage V_{GH} applies a first voltage to the gate signal line Gi (figure 3A, col. 6, lines 1-45), the gate low voltage V_{GL} applied a second voltage to the gate line Gi sequentially (figure 3B, col. 6, lines 46-58), the gate driver 3 supplied the gate buses G1, G2, ...,Gm+1 one after another with pulse-like scanning voltages Vg1, VG2, ...,VGm+1 one horizontal scanning period H and are sequentially displaced one horizontal scanning period apart in phase (col.4, lines 53-59). In figure 7, it is also possible to generate voltage K1 (Vx1+Vx2) and K2 (Vx1-Vx2) from the first and second voltage variable voltage source 6 and 7. It must be noted that the bias voltage Vx1 and Vx2 are provided immediately prior to the application of the gate select level V_{GH} (a first gate voltage changing prior to exiting of successive gate signal lines as claimed, col. 4, lines 15-17).

As to claim 10-15, Yasui teaches the generate voltage K1 (Vx1+Vx2) and K2 (Vx1-Vx2) from the first and second voltage variable voltage source 6 and 7. It must be noted that the bias voltage Vx1 and Vx2 are provided immediately prior to the application of the gate select level V_{GH} (a first gate voltage changing prior to exiting of successive gate signal lines as claimed, figure 7, col. 4, lines 15-17). Yasui teaches an

equivalent circuit diagram for explaining the migration of charges at the time when a TFT (switch) is in the ON state in Fig. 1B and the ground (the voltage controller as claimed, as claimed, col. 3, lines 46-48). An equivalent circuit diagram for explaining the migration of changes at the time when the TFT (switch) is in the OFF state in Fig. 1B and the ground (the voltage controller, as claimed, col. 3, lines 49-51).

As claim 16, Yasui et al teaches an active matrix liquid crystal display device having a plurality of pixels Lij (figure 1B), a source driver 2 connecting to n columns of source driver Si-Sn, and a gate driver 3 connecting to m+1 rows of gate buses Gi-Gm+1 (col. 4, lines 31-33).

The gate high voltage V_{GH} applies a first voltage to the gate signal line Gi (figure 3A, col. 6, lines 1-45), the gate low voltage V_{GL} applied a second voltage to the gate line Gi sequentially (figure 3B, col. 6, lines 46-58), the gate driver 3 supplied the gate buses G1, G2,...,Gm+1 one after another with pulse-like scanning voltages Vg1, VG2, ...,VGm+1 one horizontal scanning period H and are sequentially displaced one horizontal scanning period apart in phase (col.4, lines 53-59). In figure 7, it is also possible to generate voltage K1 (Vx1+Vx2) and K2 (Vx1-Vx2) from the first and second voltage variable voltage source 6 and 7. It must be noted that the bias voltage Vx1 and Vx2 are provided immediately prior to the application of the gate select level V_{GH} (a first gate voltage changing prior to exiting of successive gate signal lines as claimed, col. 4, lines 15-17).

An equivalent circuit diagram for explaining the migration of charges at the time when a TFT is in the ON state in Fig. 1B (the first control voltage connect the first

electrode with the pixel electrode as claimed, col. 3, lines 46-48). An equivalent circuit diagram for explaining the migration of changes at the time when the TFT is in the OFF state in Fig. 1B (the second control voltage disconnect the first electrode from the pixel electrode as claimed, col. 3, lines 49-51).

As to claim 17, Yasui teaches the generate voltage K1 (Vx1+Vx2) and K2 (Vx1-Vx2) from the first and second voltage variable voltage source 6 and 7. It must be noted that the bias voltage Vx1 and Vx2 are provided immediately prior to the application of the gate select level V_{GH} (figure 7, col. 4, lines 15-17).

As to claim 18, Yasui teaches the high level voltage and a ground voltage (fixed voltage) prior to the gate driver 3 (figure 3A and 3B).

As to claims 19 and 20, Yasui teaches an equivalent circuit diagram for explaining the migration of charges at the time when a TFT is in the ON state in Fig. 1B (the first control voltage connect the first electrode with the pixel electrode as claimed, col. 3, lines 46-48). An equivalent circuit diagram for explaining the migration of changes at the time when the TFT is in the OFF state in Fig. 1B (the second control voltage disconnect the first electrode from the pixel electrode as claimed, col. 3, lines 49-51).

As to claim 21, Yasui et al teaches a method of an active matrix liquid crystal display device having a plurality of pixels Lij (figure 1B), a source driver 2 connecting to n columns of source driver Si-Sn, and a gate driver 3 connecting to m+1 rows of gate buses Gi-Gm+1 (col. 4, lines 31-33).

The gate high voltage V_{GH} applies a first voltage to the gate signal line Gi (figure 3A, col. 6, lines 1-45), the gate low voltage V_{GL} applied a second voltage to the gate line Gi sequentially (figure 3B, col. 6, lines 46-58), the gate driver 3 supplied the gate buses G1, G2, ...,Gm+1 one after another with pulse-like scanning voltages Vg1, VG2, ...,VGm+1 one horizontal scanning period H and are sequentially displaced one horizontal scanning period apart in phase (col.4, lines 53-59). In figure 7, it is also possible to generate voltage K1 (Vx1+Vx2) and K2 (Vx1-Vx2) from the first and second voltage variable voltage source 6 and 7. It must be noted that the bias voltage Vx1 and Vx2 are provided immediately prior to the application of the gate select level V_{GH} (a first gate voltage changing prior to exiting of successive gate signal lines as claimed, col. 4, lines 15-17).

An equivalent circuit diagram for explaining the migration of charges at the time when a TFT is in the ON state in Fig. 1B (the first control voltage connect the first electrode with the pixel electrode as claimed, col. 3, lines 46-48). An equivalent circuit diagram for explaining the migration of changes at the time when the TFT is in the OFF state in Fig. 1B (the second control voltage disconnect the first electrode from the pixel electrode as claimed, col. 3, lines 49-51).

As to claims 22-26, Yasui et al teaches figure 9 having a waveform VGH and VGL rise and fall times at leading and trailing edges of the gate pulse and the second bias voltage, respectively in Fig. 8A (col. 4, lines 15-17).

Response to Arguments

4. Applicant's arguments filed 2/14/2002 have been fully considered but they are not persuasive. See the rejections above.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-FRI from 9:00-5:00 with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600